DATA SHEET

SAA6581

RDS/RBDS demodulator

Product specification
Supersedes data of 2002 Jan 14

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Philips
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RDS/RBDS demodulator SAA6581

FEATURES

- Integrated switched capacitor filter
- Demodulates European Radio Data System (RDS) or the USA Radio Broadcast Data System (RBDS) signals
- Oscillator frequencies: 4.332 or 8.664 MHz
- Integrated ARI clamping
- CMOS device
- Single supply voltage: 5 V
- Extended temperature range: −40 to +85 °C
- Low number of external components.

APPLICATIONS

The RDS/RBDS system offers a large range of applications from the many functions that can be implemented. For car radios the most important are:

- Program Service (PS) name
- Traffic Program (TP) identification
- Traffic Announcement (TA) signal
- Alternative Frequency (AF) list
- Program Identification (PI)
- Enhanced Other Networks (EON) information.

GENERAL DESCRIPTION

The RDS/RBDS demodulator is a CMOS device with integrated filtering and demodulating of RDS/RBDS signals coming from a multiplexed input data stream. Data signal RDDA and clock signal RDCL are provided as outputs for further processing by a suitable microcomputer, for example CCR921 and CCR922.

The SAA6581T replaces SAA6579 in function and pin-compatibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.0	5.0	5.5	V
V_{DDD}	digital supply voltage	4.0	5.0	5.5	V
$I_{DD(tot)}$	total supply current	–	6.0	–	mA
$V_{i(MPX)}$	RDS input sensitivity at pin MPX	1	–	–	mV
$f_{i(xtal)}$	crystal input frequency	–	4.332	–	MHz
		–	8.664	–	MHz

ORDERING INFORMATION

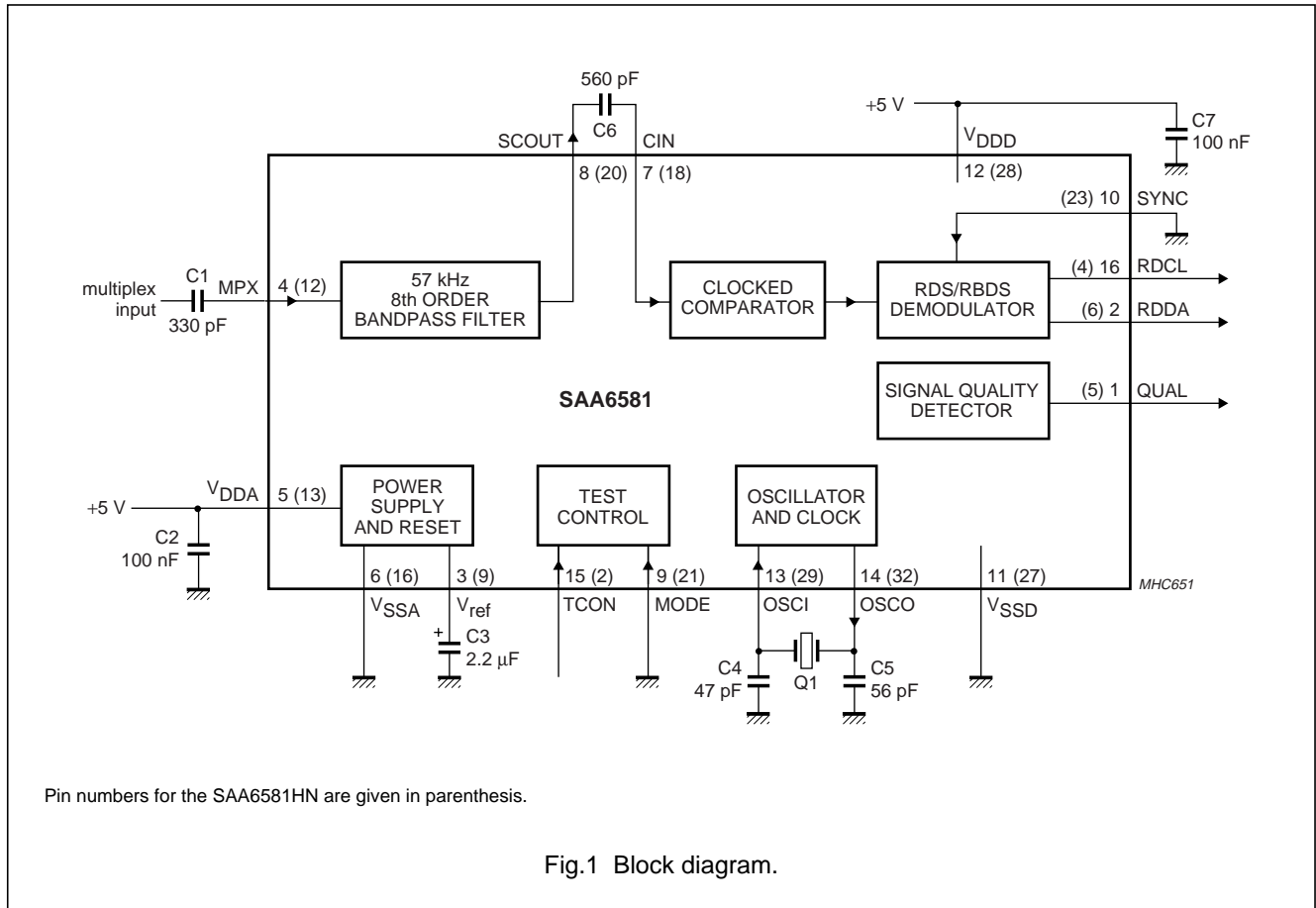| TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION		VERSION
SAA6581T	SO16	plastic small outline package; 16 leads; body width 7.5 mm		SOT162-1
SAA6581HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm		SOT617-1

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BLOCK DIAGRAM

Pin numbers for the SAA6581HN are given in parenthesis.

Fig.1 Block diagram.

RDS/RBDS demodulator

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PINNING

SYMBOL	PIN		DESCRIPTION
	SO16	HVQFN32	
QUAL	1	5	signal quality indication output
RDDA	2	6	RDS data output
n.c.	–	7	not connected
n.c.	–	8	not connected
V_{ref}	3	9	reference voltage output ($^1/_2V_{DDA}$)
n.c.	–	10	not connected
n.c.	–	11	not connected
MPX	4	12	multiplex signal input
V_{DDA}	5	13	analog supply voltage (5 V)
n.c.	–	14	not connected
n.c.	–	15	not connected
V_{SSA}	6	16	analog ground (0 V)
n.c.	–	17	not connected
CIN	7	18	comparator input
n.c.	–	19	not connected
SCOUT	8	20	switched capacitor filter output

| SYMBOL	PIN		DESCRIPTION
	SO16	HVQFN32	
MODE	9	21	oscillator frequency select input
n.c.	–	22	not connected
SYNC	10	23	ARI clamping control input
n.c.	–	24	not connected
n.c.	–	25	not connected
n.c.	–	26	not connected
V_{SSD}	11	27	digital ground (0 V)
V_{DDD}	12	28	digital supply voltage (5 V)
OSCI	13	29	oscillator input
n.c.	–	30	not connected
n.c.	–	31	not connected
OSCO	14	32	oscillator output
n.c.	–	1	not connected
TCON	15	2	test control input
n.c.	–	3	not connected
RDCL	16	4	RDS clock output
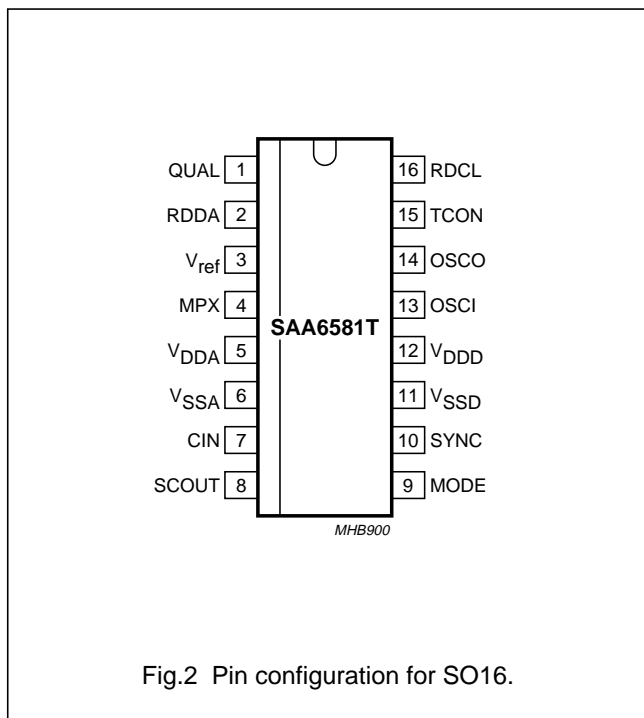
Fig.2 Pin configuration for SO16.
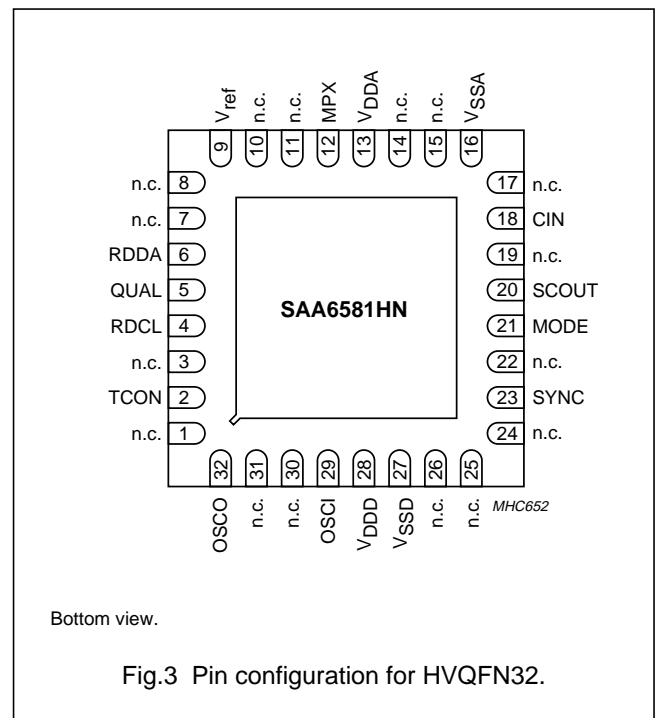
Fig.3 Pin configuration for HVQFN32.

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FUNCTIONAL DESCRIPTION

RDS/RBDS signal demodulation

BANDPASS FILTER

The bandpass filter has a centre frequency of 57 kHz. It selects the RDS/RBDS sub-band from the multiplex signal MPX and suppresses the audio signal components. The filter block contains an analog anti-aliasing filter at the input followed by an 8th order switched capacitor bandpass filter and a reconstruction filter at the output.

CLOCKED COMPARATOR

The comparator digitizes the output signal from the 57 kHz bandpass filter for further processing by the digital RDS/RBDS demodulator. To attain high sensitivity and to avoid phase distortion, the comparator input stage has automatic offset compensation.

DEMODULATOR

The demodulator provides all functions of the SAA6579 and improves performance under weak signal conditions.

Demodulator functions include:

- 57 kHz carrier regeneration from the two sidebands (Costas loop)
- Symbol integration over one RDS clock period
- Bi-phase symbol decoding
- Differential decoding
- Synchronization of RDS/RBDS output data.

The RDS/RBDS demodulator recovers and regenerates the continuously transmitted RDS/RBDS data stream in the MPX signal and provides clock RDCL for the output signals and data output RDDA for further processing by an RDS/RBDS decoder, for example CCR921 or CCR922.

ARI CLAMP

The demodulator checks the input signal for presence of RDS only, or RDS plus ARI transmissions. After a fixed test period, if the SYNC input is set HIGH the demodulator locks in the 'verified' condition (see Table 1). If SYNC is set LOW, the ARI clamping is reset (disabled). After SYNC returns to HIGH, the demodulator resumes checking the input signal.

Table 1   Control pin SYNC

SYNC	ARI CLAMPING
LOW	internal ARI clamping disabled
HIGH	ARI clamping allowed to be logged

SIGNAL QUALITY DETECTION

Output QUAL indicates the safety of the regenerated RDS data (HIGH = 'good' data; LOW = 'unsafe' data).

Oscillator and system clock generator

For good performance of the bandpass and demodulator stages, the demodulator requires a crystal oscillator with a frequency of 4.332 or 8.664 MHz. The demodulator can operate with either frequency (see Table 2), so that a radio set with a microcontroller can run, in this case, with one crystal only. The demodulator oscillator can drive the microcontroller, or vice versa.

Table 2   Control pins TCON and MODE

TCON	MODE	OSCILLATOR FREQUENCY
HIGH	LOW	4.332 MHz
HIGH	HIGH	8.664 MHz

The clock generator generates the internal 4.332 MHz system clock and timing signal derivatives.

Power supply and internal reset

The demodulator has separate power supply inputs for the digital and analog parts of the device. For the analog functions an additional reference voltage ($\frac{1}{2}V_{DDA}$) is internally generated and available via the output pin V_{ref}. The demodulator requires a defined reset condition. The demodulator generates automatically a reset signal after the power supply V_{DDA} is switched on, or at a voltage-drop.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	6.5	V
V_n	voltage at pins QUAL, RDDA, V_{ref}, MPX, CIN, SCOUT, MODE, SYNC, OSCI, OSCO, TCON and RDCL with respect to pins V_{SSA} and V_{SSD}	pins V_{DDA} and V_{DDD} are connected to V_{DD}	−0.5	$V_{DD} + 0.5 \leq 6.5$	V
$V_{i(MPX)(p-p)}$	input voltage at pin MPX (peak-to-peak value)	note 1	−	6	V
I_i	input current at pins QUAL, RDDA, V_{ref}, MPX, V_{DDA}, CIN, SCOUT, MODE, SYNC, V_{DDD}, OSCI, OSCO, TCON and RDCL	pins V_{SSA} and V_{SSD} are connected to ground	−10	+10	mA
$I_{lu(prot)}$	latch-up protection current in pulsed mode	T_{amb} = −40 to +85 °C with voltage limiting −2 to +10 V	−100	+100	mA
		T_{amb} = 25 °C with voltage limiting −2 to +12 V	−200	+200	mA
		T_{amb} = −40 to +85 °C without voltage limiting	−10	+10	mA
T_{amb}	ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling voltage	note 2	−3000	+3000	V
		note 3	−400	+400	V

Notes

1. Without latching in the entire temperature range.

2. Human body model (equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

3. Machine model (equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor and 0.75 µH inductance).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SAA6581T (SO16)		104	K/W
	SAA6581HN (HVQFN32)	with soldered heatsink	100	K/W

CHARACTERISTICS: DIGITAL PART

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.0	5.0	5.5	V
I_{DDD}	digital supply current		–	1.5	–	mA
P_{tot}	total power dissipation		–	30	–	mW
Inputs						
V_{IL}	LOW-level input voltage at pins TCON, OSCI, SYNC and MODE		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage at pins TCON, OSCI, SYNC and MODE		$0.7V_{DDD}$	–	–	V
$I_{i(pu)}$	input pull-up current at pins TCON and MODE	$V_{IH} = 3.5$ V	−10	−20	–	µA
Outputs						
V_{OL}	LOW-level output voltage at pins QUAL, RDDA and RDCL	$I_{OL} = 2$ mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage at pins QUAL, RDDA and RDCL	$I_{OH} = -0.02$ mA	4.0	–	–	V
Crystal parameters						
$f_{i(xtal)}$	crystal input frequency	TCON = HIGH; MODE = LOW	–	4.332	–	MHz
		TCON = HIGH; MODE = HIGH	–	8.664	–	MHz
$\|\Delta f_{osc}\|$	adjustment tolerance of oscillator frequency		–	–	30×10^{-6}	
$\|\Delta f_{osc(T)}\|$	temperature drift of oscillator frequency	$T_{amb} = -40$ to $+85$ °C	–	–	30×10^{-6}	
C_L	load capacitance		–	30	–	pF
R_{xtal}	crystal resonance resistance		–	–	120	Ω

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CHARACTERISTICS: ANALOG PART

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; measurements taken in Fig.1; unless otherwise specified.

| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.0	5.0	5.5	V
$\|V_{DDA} - V_{DDD}\|$	difference between analog and digital supply voltages		–	0	0.5	V
$I_{DD(tot)}$	total supply current		–	6.0	–	mA
V_{ref}	reference voltage	$V_{DDA} = 5$ V	2.25	2.5	2.75	V
$Z_{o(Vref)}$	output impedance at pin V_{ref}		–	25	–	kΩ
MPX input (signal before the capacitor on pin MPX)						
$V_{i(MPX)(rms)}$	RDS amplitude (RMS value)	$\Delta f = \pm1.2$ kHz RDS-signal; $\Delta f = \pm3.2$ kHz ARI-signal	1	–	–	mV
$V_{i(max)(p-p)}$	maximum input signal capability (peak-to-peak value)	$f = 57 \pm2$ kHz	200	–	–	mV
		$f < 50$ kHz	1.4	–	–	V
		$f < 15$ kHz	2.8	–	–	V
		$f > 70$ kHz	3.5	–	–	V
$R_{i(MPX)}$	input resistance	$f = 0$ to 100 kHz	40	–	–	kΩ
57 kHz bandpass filter						
f_c	centre frequency	$T_{amb} = -40$ to +85 °C	56.5	57.0	57.5	kHz
B_{-3dB}	−3 dB bandwidth		2.5	3.0	3.5	kHz
$G_{SCOUT-MPX}$	signal gain	$f = 57$ kHz	17	20	23	dB
α_{sb}	stop band attenuation	$\Delta f = \pm7$ kHz	31	–	–	dB
		$f < 45$ kHz	40	–	–	dB
		$f < 20$ kHz	50	–	–	dB
		$f > 70$ kHz	40	–	–	dB
$R_{o(SCOUT)}$	output resistance at pin SCOUT	$f = 57$ kHz	–	30	60	Ω
Comparator input (pin CIN)						
$V_{i(min)(rms)}$	minimum input level (RMS value)	$f = 57$ kHz	–	1	10	mV
R_i	input resistance		70	110	150	kΩ

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TIMING DATA
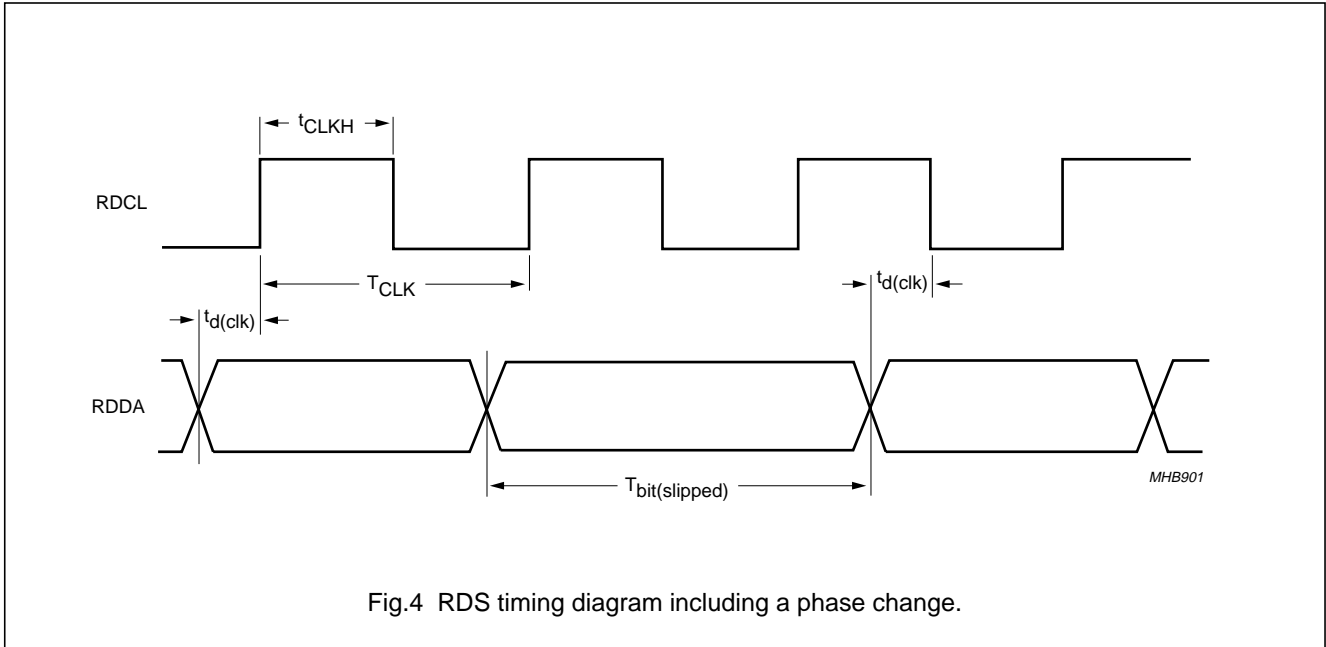
Fig.4 RDS timing diagram including a phase change.

Table 3 RDS timing (see Fig.4)

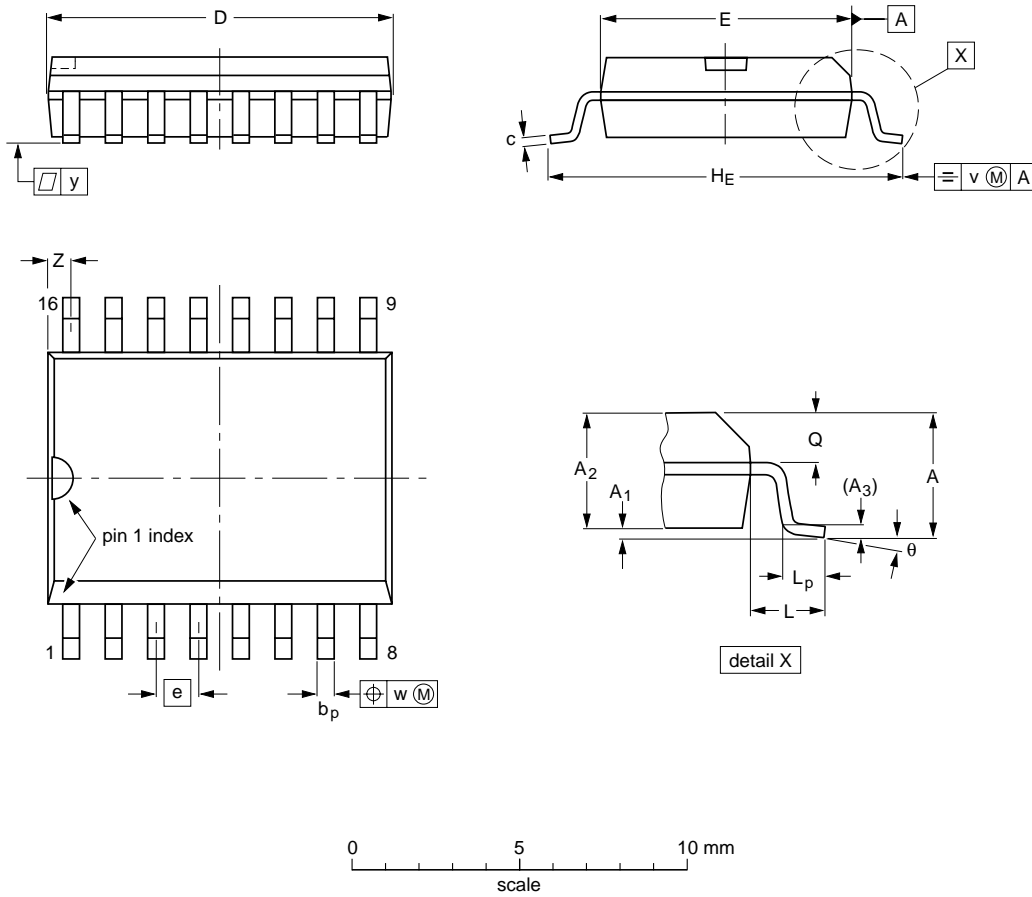| SYMBOL	PARAMETER	TYP.	UNIT
$t_{d(clk)}$	clock-data delay	4	µs
T_{CLK}	clock period	842	µs
t_{CLKH}	clock HIGH time	421	µs
$T_{bit(slipped)}$	slipped data bit period	1263	µs

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

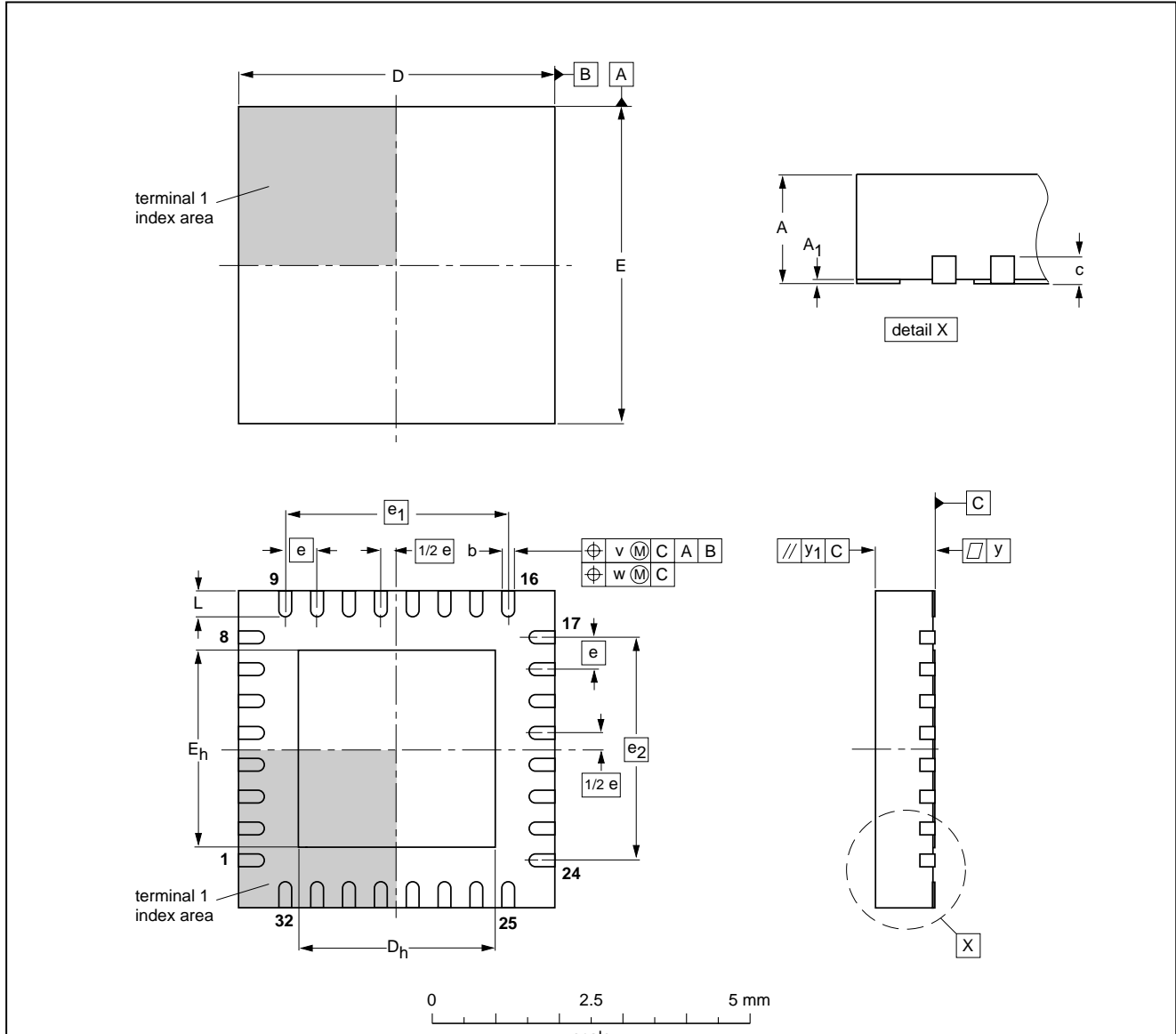1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				99-12-27 03-02-19

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**HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;
32 terminals; body 5 x 5 x 0.85 mm**

SOT617-1

DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A₁	b	c	D(1)	Dₕ	E(1)	Eₕ	e	e₁	e₂	L	v	w	y	y₁
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

• below 220 °C (SnPb process) or below 245 °C (Pb-free process)

 – for all the BGA and SSOP-T packages

 – for packages with a thickness ≥ 2.5 mm

 – for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.

• below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

• Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

• For packages with leads on two sides and a pitch (e):

 – larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

 – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

 The footprint must incorporate solder thieves at the downstream end.

• For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe

dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	suitable
Through-hole-surface mount	PMFP[9]	not suitable	not suitable	–
Surface mount	BGA, LBGA, LFBGA, SQFP, SSOP-T[4], TFBGA, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[5]	suitable	–
	PLCC[6], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[6][7]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[8]	suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.

2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

4. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

5. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

6. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

7. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

8. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

9. Hot bar soldering or manual soldering is suitable for PMFP packages.

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.

2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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